AMENDMENTS TO THE CLAIMS

No claim amendments have been made in this response. This listing is included for the examiner's convenience and will replace all prior versions, and listings, of claims in the application:

Claim 1 (original): A semiconductor memory device including a plurality of memory cells, wherein one of the plurality of memory cells includes a variable resistor having a resistance value thereof reversibly changed in accordance with a voltage applied thereto, and a transistor connected to the variable resistor.

Claim 2 (original): A semiconductor memory device according to claim 1, wherein the transistor is a MOS transistor.

Claim 3 (original): A semiconductor memory device according to claim 1, wherein the resistance value of the variable resistor is set to reach a plurality of non-overlapping ranges.

Claim 4 (original): A semiconductor memory device according to claim 1, wherein the variable resistor is formed of a material having a perovskite type crystalline structure.

Claim 5 (original): A semiconductor memory device according to claim 1, wherein:

the transistor includes a source, a gate, and a drain, and

one of the source and the drain is connected to a bit line via the variable resistor, and the gate is connected to a word line.

Claim 6 (original): A semiconductor memory device according to claim 5, wherein a

voltage of a prescribed polarity is applied to the bit line, and a voltage lower than the voltage of the prescribed polarity is applied to the word line, so that the one memory cell is selected from the plurality of memory cells and data is written to the one memory cell.

Claim 7 (original): A semiconductor memory device according to claim 6, wherein a voltage of a polarity opposite to the prescribed polarity is applied to the bit line, and a voltage lower than the voltage of the prescribed polarity is applied to the word line, so that the one memory cell is selected from the plurality of memory cells and data is erased from the one memory cell.

Claim 8 (original): A data write method for writing data to a memory cell, wherein the memory cell includes a variable resistor having a resistance value thereof reversibly changed in accordance with a voltage applied thereto, and a transistor connected to the variable resistor, the data write method comprising:

a first step of applying a first data write voltage to the memory cell;

a second step of, after the first data write voltage is applied, determining whether or not the resistance value of the variable resistor is within a prescribed range;

a third step of, when the resistance value of the variable resistor has not reached the prescribed range, applying a second data write voltage which is higher than the first data write voltage to the memory cell; and

a fourth step of repeating the second step and the third step until the resistance value of the variable resistor reaches the prescribed range.

Claim 9 (original): A data write method according to claim 8, further comprising:

a fifth step of, when the resistance value of the variable resistor exceeds the prescribed range, applying a data erase voltage to the variable resistor;

a sixth step of, after the data erase voltage is applied, determining whether or not the resistance value of the variable resistor has reached a data erase range; and

a seventh step of repeating the fifth step and the sixth step until the resistance value of the variable resistor reaches the data erase range and then applying the first data write voltage to the memory cell.

Claim 10 (original): A data write method according to claim 8, wherein the third step includes a step of applying the second data write voltage in a time period which is shorter than a time period in which the first data write voltage is applied in the first step.